Survey on

DPM (dynamic power management)
Introduction

- Dynamic power management (DPM) saves power by shutting down idle devices

- In DPM system, the state of operation of various components is dynamically adapted to the required performance level, in an effort to minimize the power wasted by idle or underutilized Components.

- For most system components, state transitions have nonnegligible power and performance costs.
Different embodiments according to the level where DPM is applied

- Component
- System
- Network
State Transitions

- Shut down
- Wake up

- Requests
- Idle
- Working
- Sleeping

- Time before shutdown
- Shutdown delay
- Sleep time
- Wakeup delay
An abstract structure of a system-level power manager.

*DPM scheme requires modeling both the components’ power/performance behavior and their workload.*
PaperClip hardware diagram

- Flash
- SRAM
- Real-time clock
- LCD display
- FPGA
- Digitizer
- CPU
- Battery stack
- Battery to 5V conv
- All 5V components
- All 12V components
- 5 to 12V conv
Classification

- Predictive Schemes
  1) static techniques
     - Fixed timeout
     - Predictive shutdown
     - Predictive wakeup
  2) Adaptive techniques

- Stochastic optimum control
  1) static techniques
     - Based on Markov models
  2) Adaptive techniques
     - Based on policy precharacterization, parameter learning, and policy interpolation
It is very possible to design our own DPM!
Hardware Restriction

- Battery Power
  - Capacity
  - Volume
  - OS should provide power management mechanisms
Hardware Restriction

- Processing Power
  - OMAP L-137
  - ARM926EJ-S + TMS320C6747
  - Freq: 300MHz
Hardware Restriction

- **Memory**
  - MMU included in ARM core
  - 32K L1P/32K L1D/256K L2 RAM/1024 L2 ROM
- **External Memory Interfaces**
  - EMIFA: 16bit SDRAM with 128MB Address Space
  - EMIFB: 16/32 bit SDRAM with 256MB Address Space
Other Problems

- ARM/DSP communication
  - Interrupts
  - Shared Memory
  - ?